DESIGNING METHOD FOR CLOCK WIRING

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Abstract

PURPOSE: To obtain a clock wiring layout which is uniform in rise/fall time at a terminal and small in skew. CONSTITUTION: After a tree type clock wiring layout is temporarily designed by a zero schema merging method (step S1), a point where the rise/fall time of a clock is less than a permissible value is found by a terminal circuit on the tree if the rise/fall time of the clock exceeds the permissible value (steps S2-S4), and a buffer amplifier is inserted there (step S5). Then, wiring layout information on the higher-order than or upstream side from a trf-allowing point is discarded (step S6) and the delay of the tree on the lower-order than or downstream side from the trf-allowing point is considered to design a tree type layout again by the zero schema merging method (step S7), and it is judged whether or not the rise/fall time of the clock at the buffer insertion point exceeds the permissible value and if the permissible value is exceeded, a buffer amplifier is inserted at the trf-allowing point, thus repeating the procedure.